FIG. 1

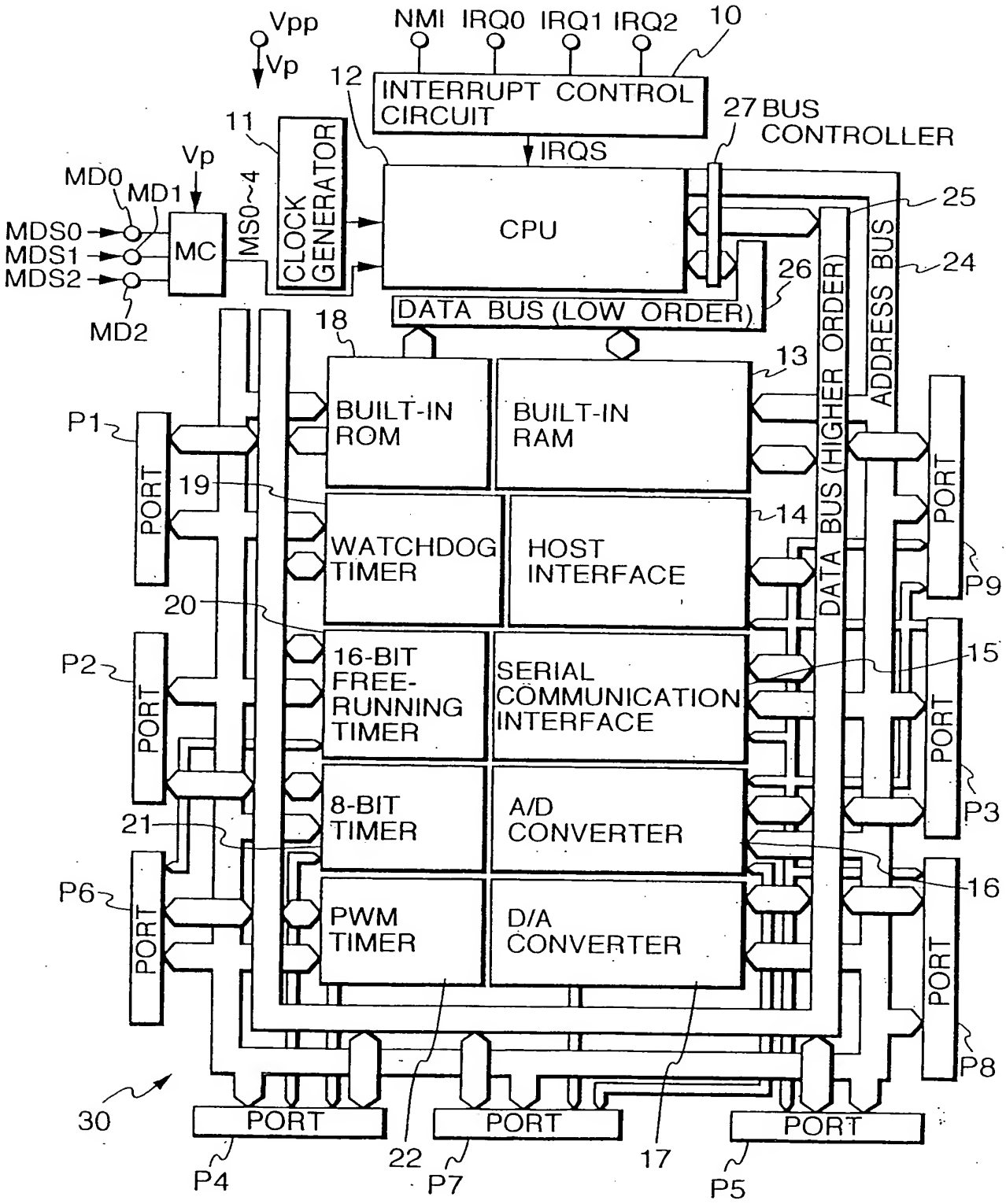


FIG. 2

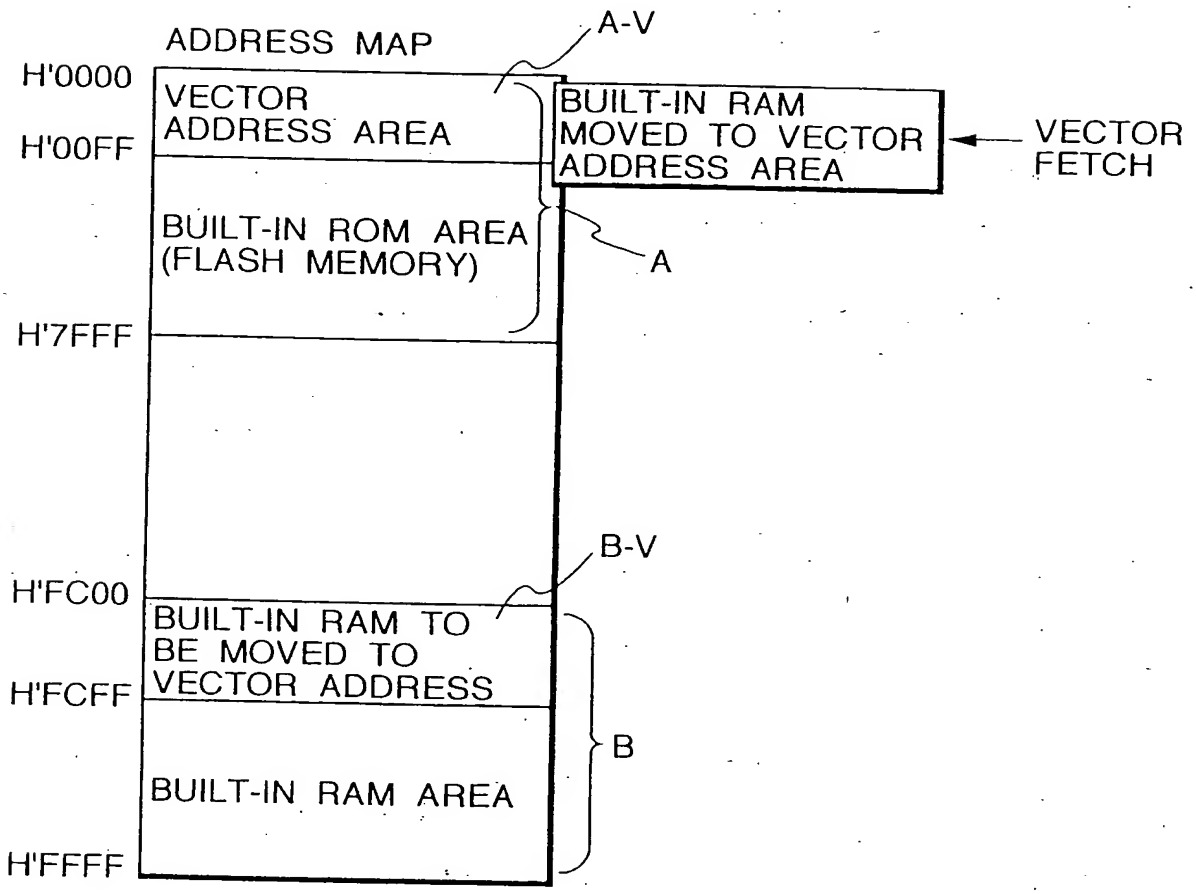


FIG. 3

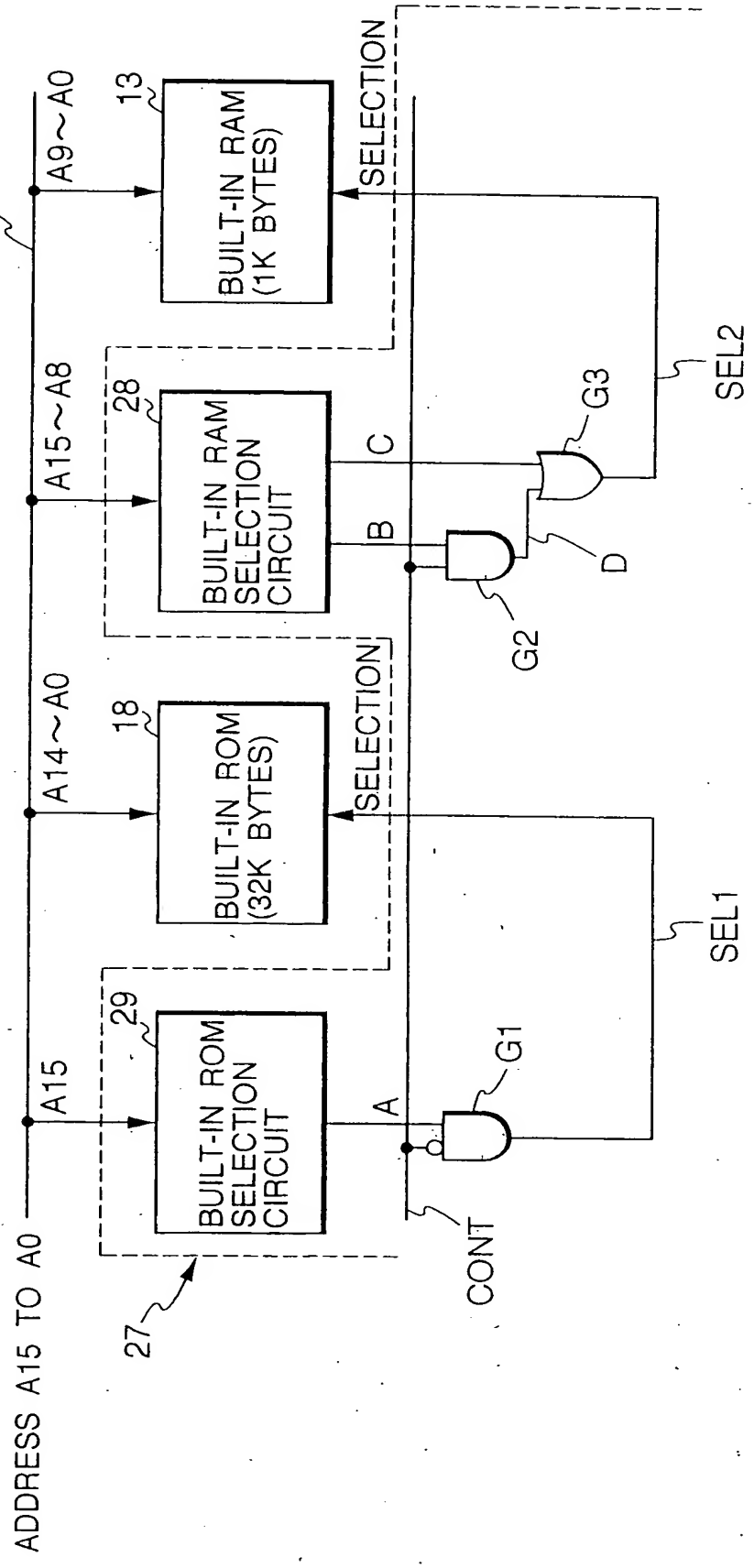


FIG. 4

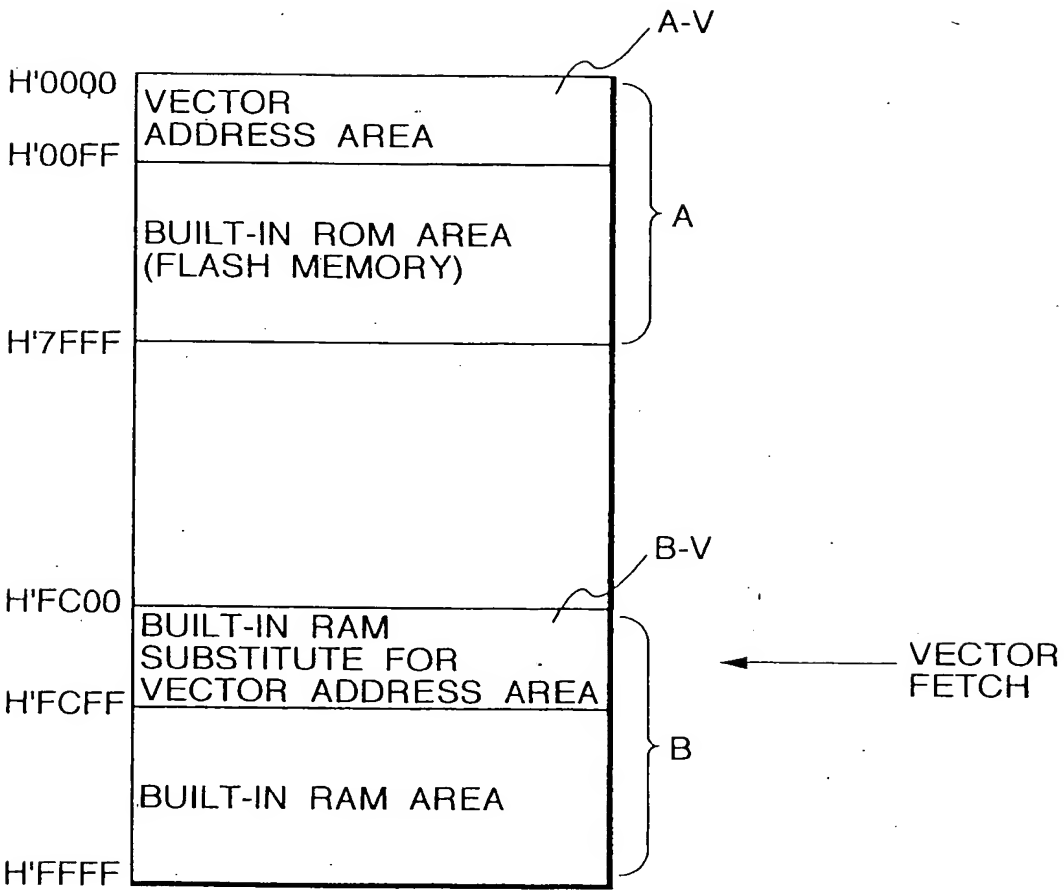


FIG. 5

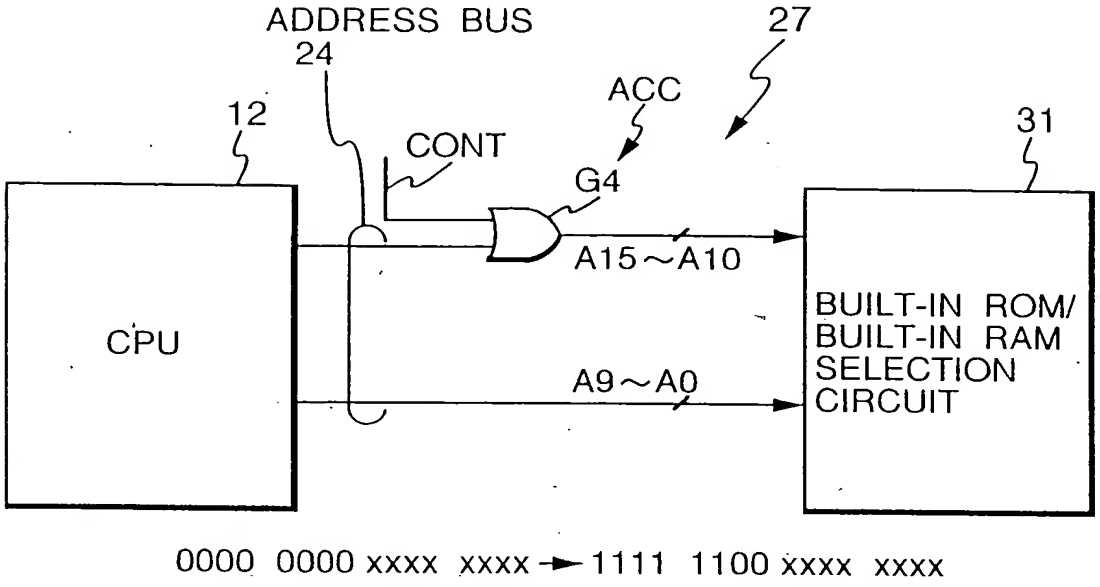


FIG. 6

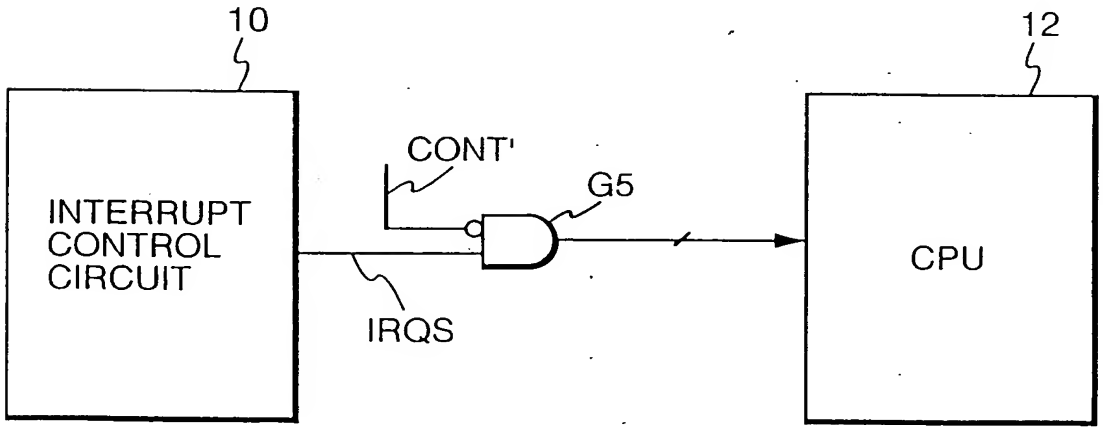


FIG. 7

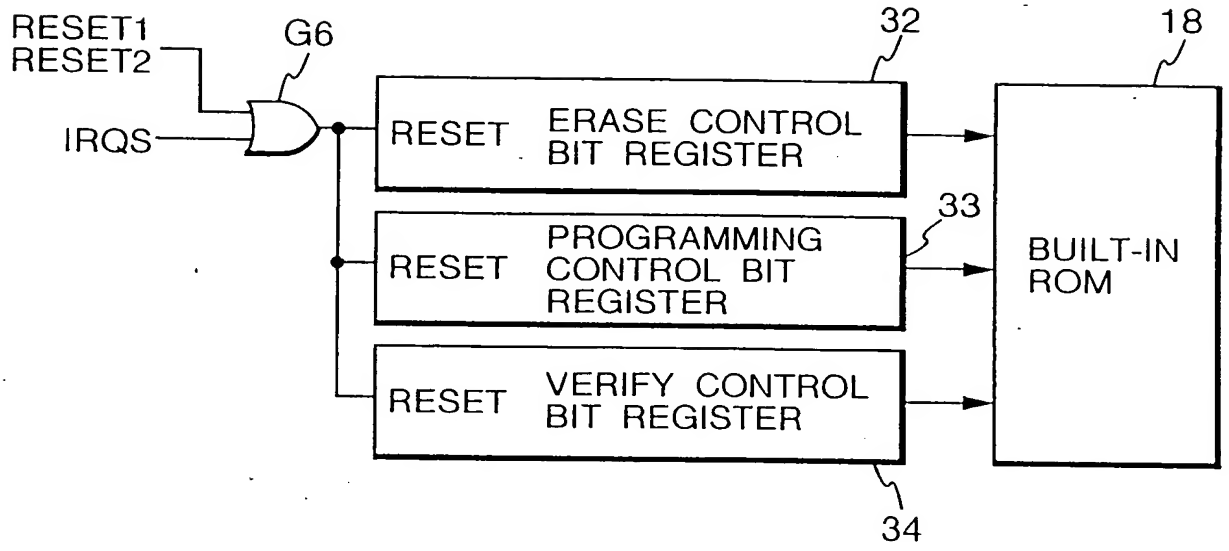


FIG. 8

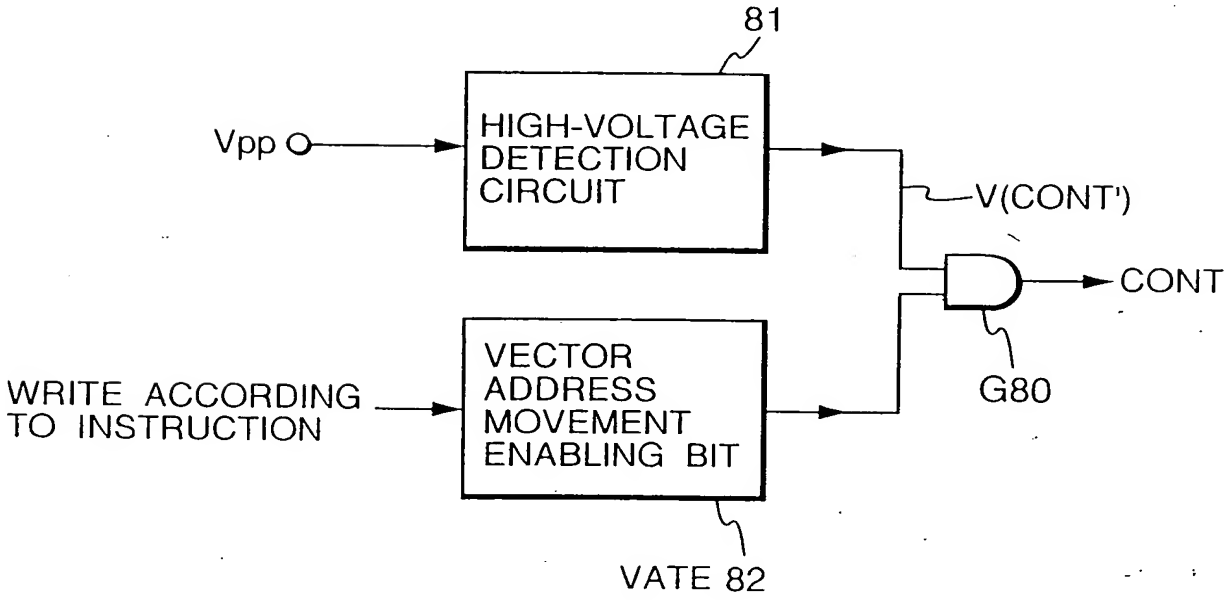


FIG. 9

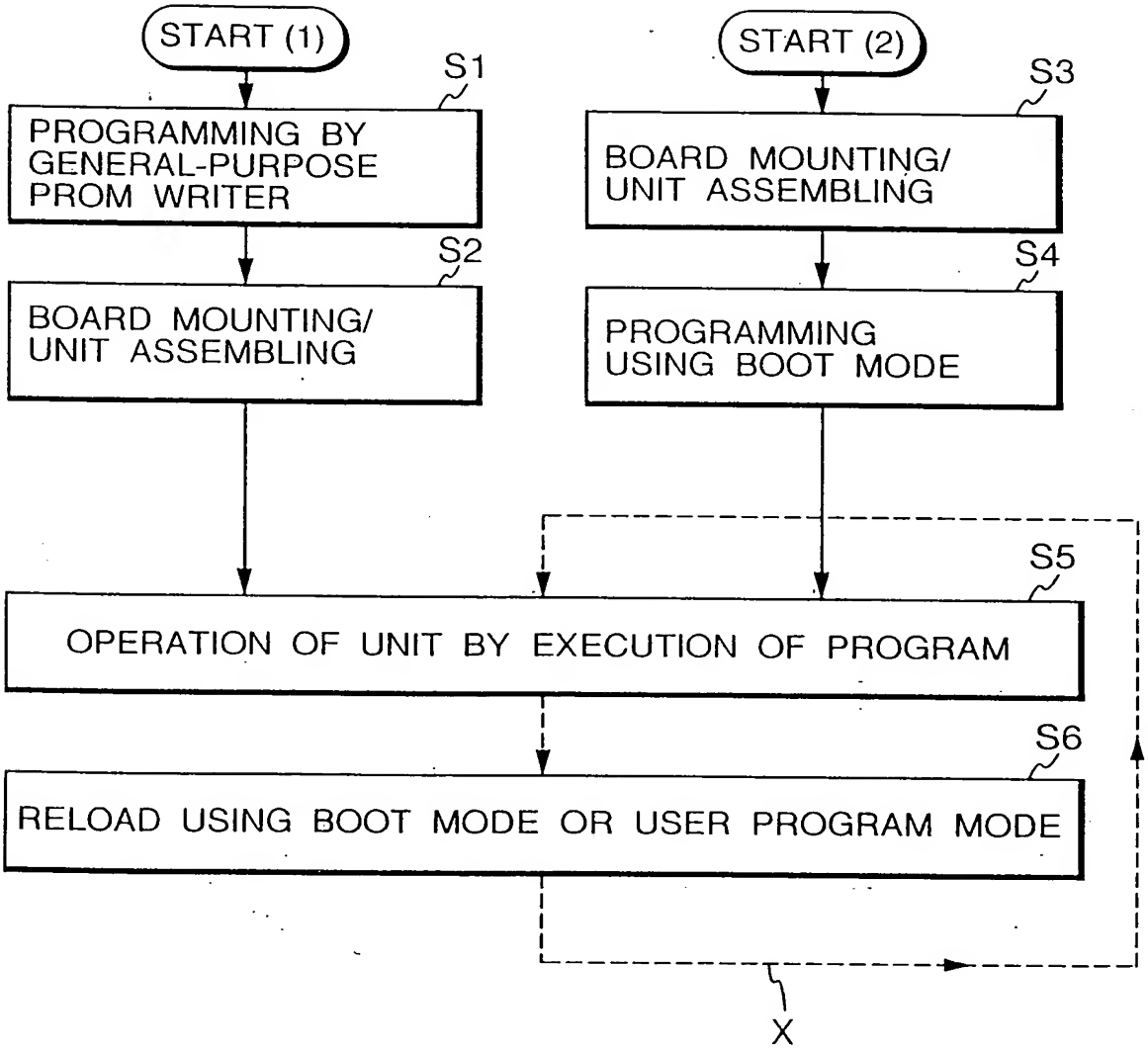
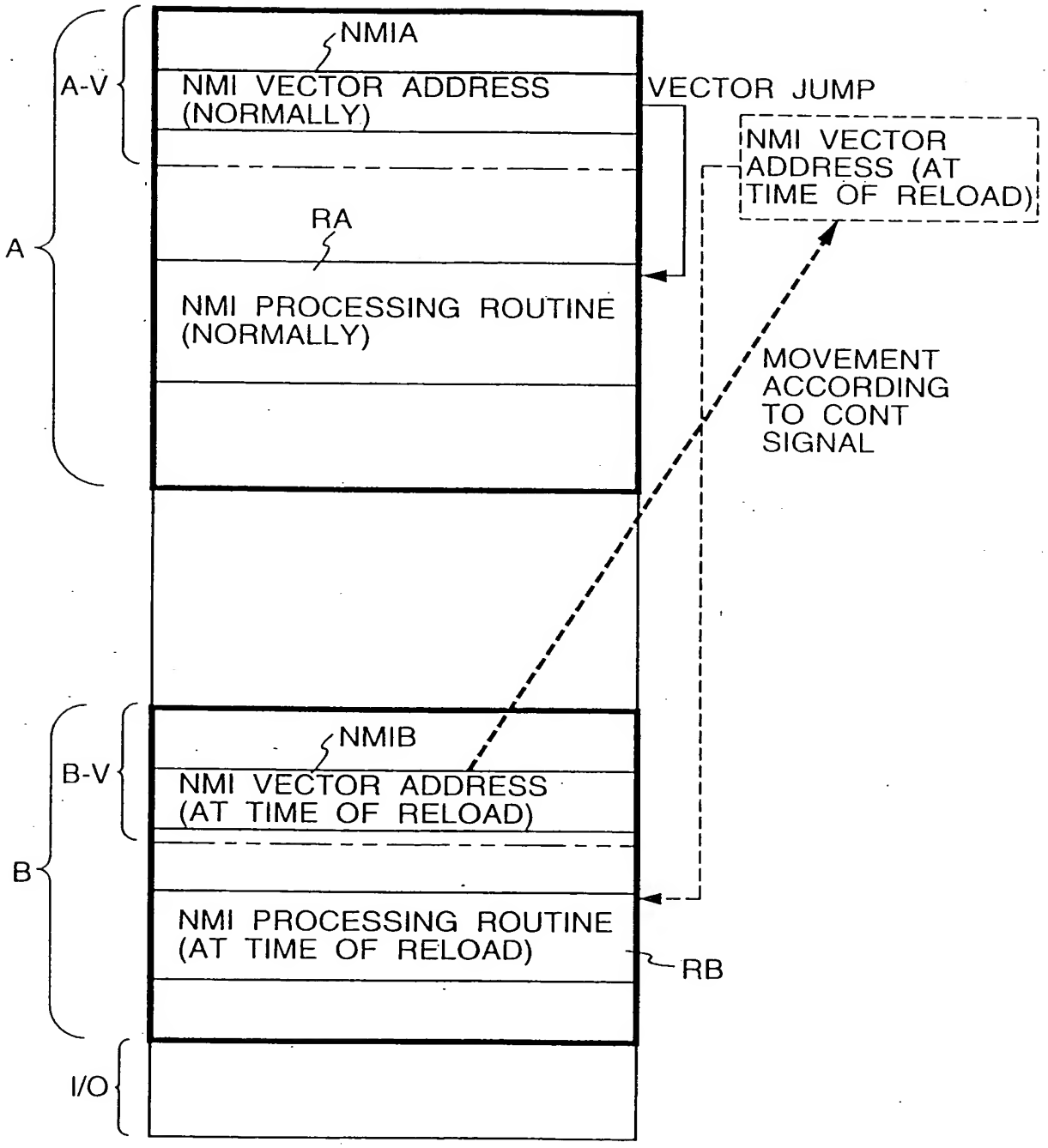


FIG. 10



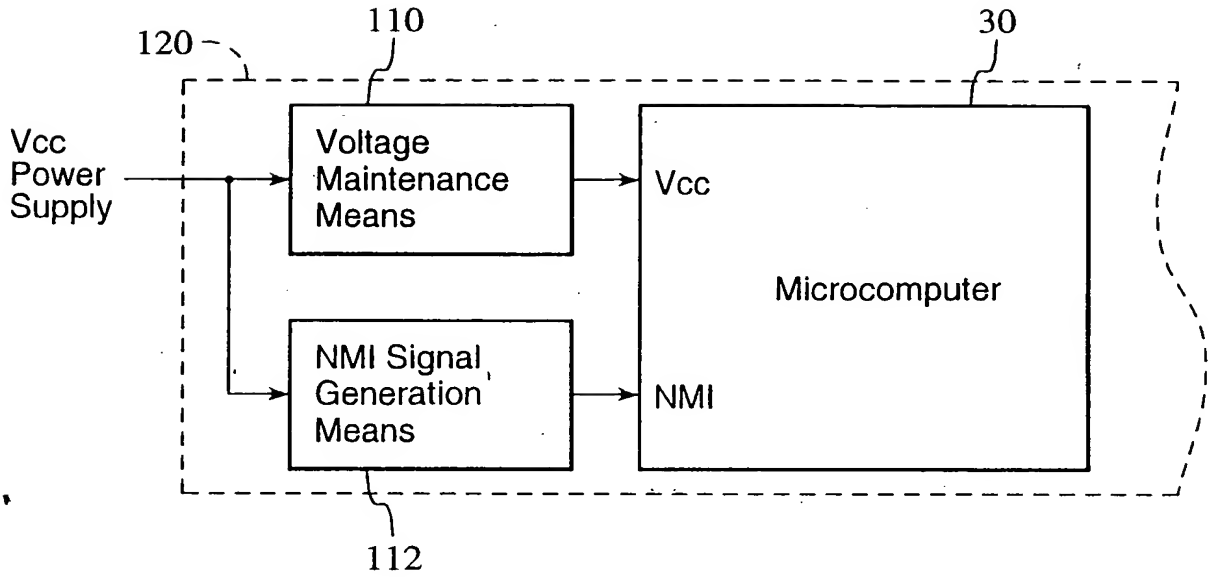


FIG. 11

PRINCIPLE OF FLASH MEMORY

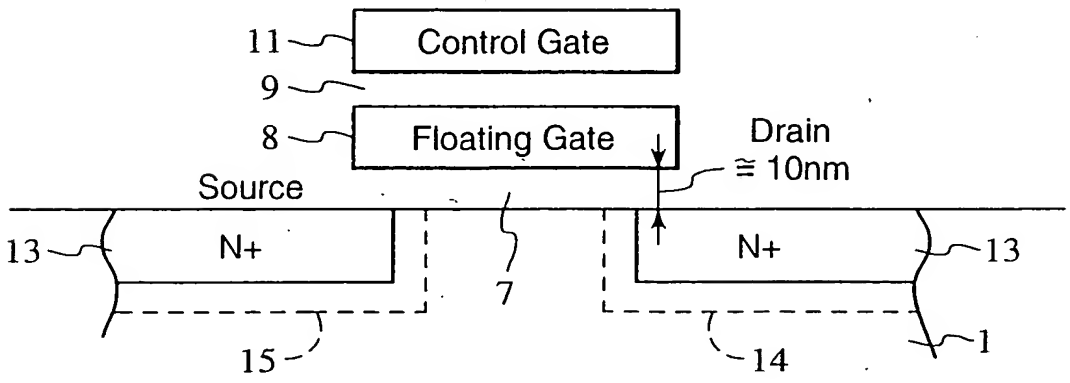


FIG. 13

FIG. 12

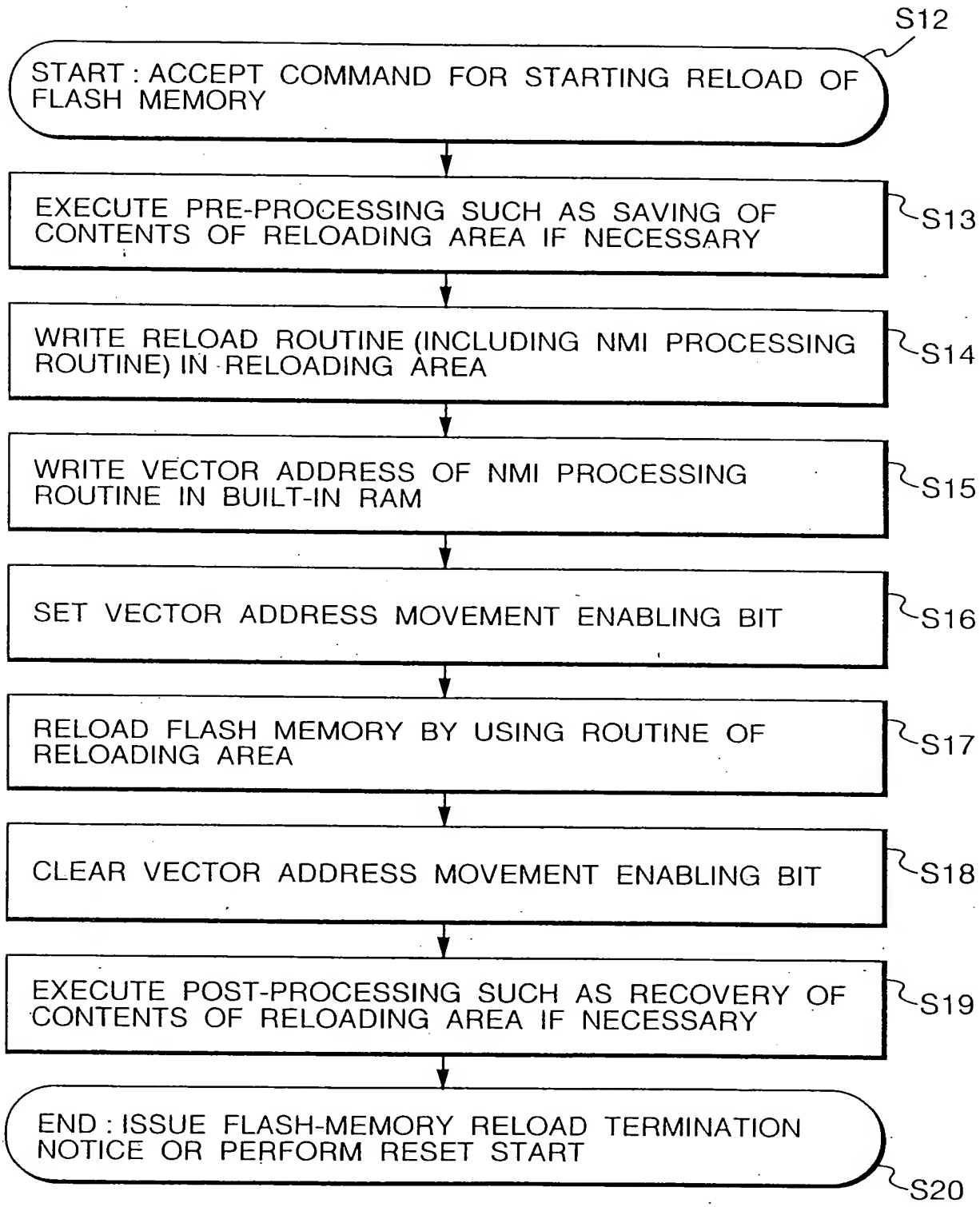


FIG. 14

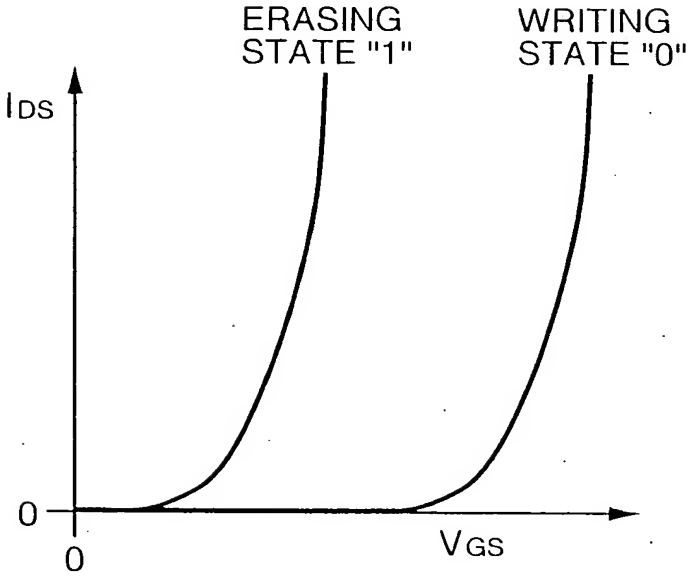


FIG. 15

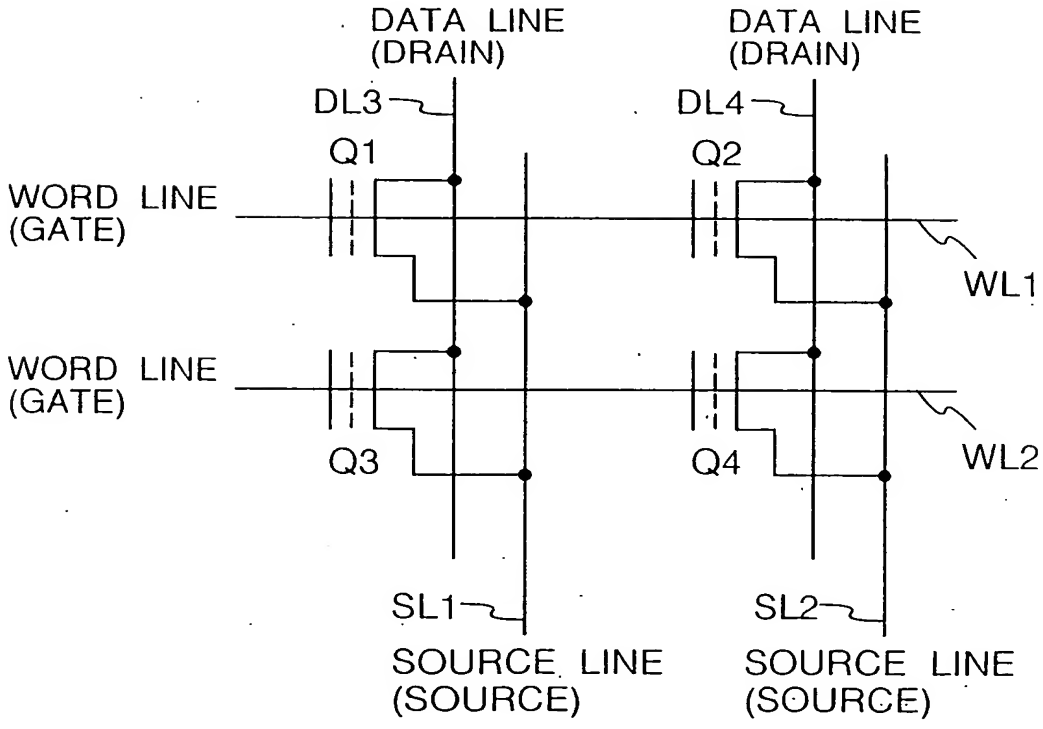


FIG. 16

WRITE

MEMORY DEVICE	SELECTIVE/ NON-SELECTIVE	SOURCE	DRAIN	GATE
Q1	SELECTIVE	0v	6v	12v
Q2	NON-SELECTIVE	0v	0v	12v
Q3	NON-SELECTIVE	0v	6v	0v
Q4	NON-SELECTIVE	0v	0v	0v

ERASE (POSITIVE VOLTAGE SYSTEM)

MEMORY DEVICE	SELECTIVE/ NON-SELECTIVE	SOURCE	DRAIN	GATE
Q1,Q3	SELECTIVE	12v	0v	0v
Q2,Q4	NON-SELECTIVE	0v	0v	0v

ERASE (NEGATIVE VOLTAGE SYSTEM)

MEMORY DEVICE	SELECTIVE/ NON-SELECTIVE	SOURCE	DRAIN	GATE
Q1,Q2	SELECTIVE	5v	0v	10v
Q3,Q4	NON-SELECTIVE	5v	0v	0v

FIG. 17

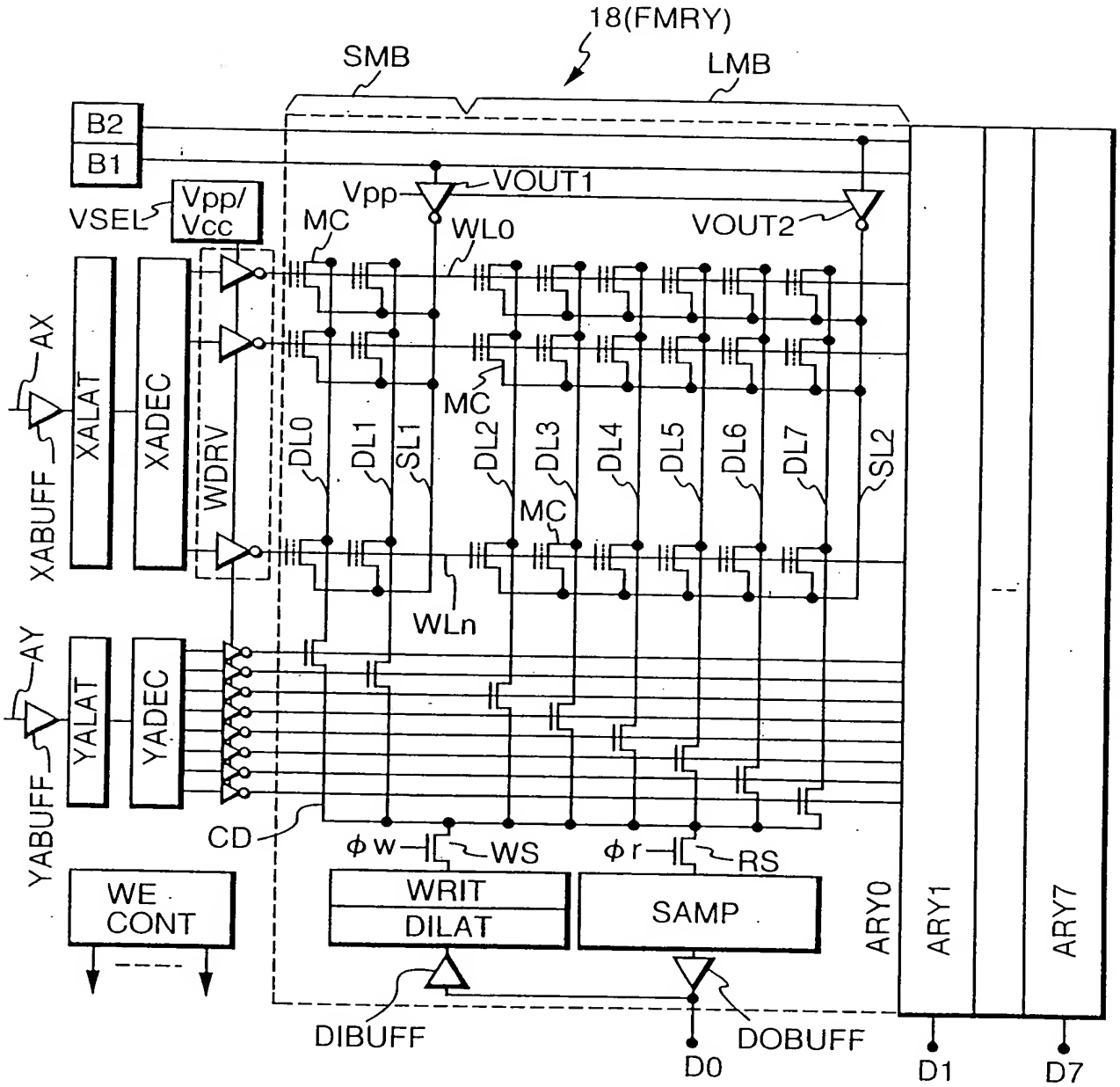


FIG. 18

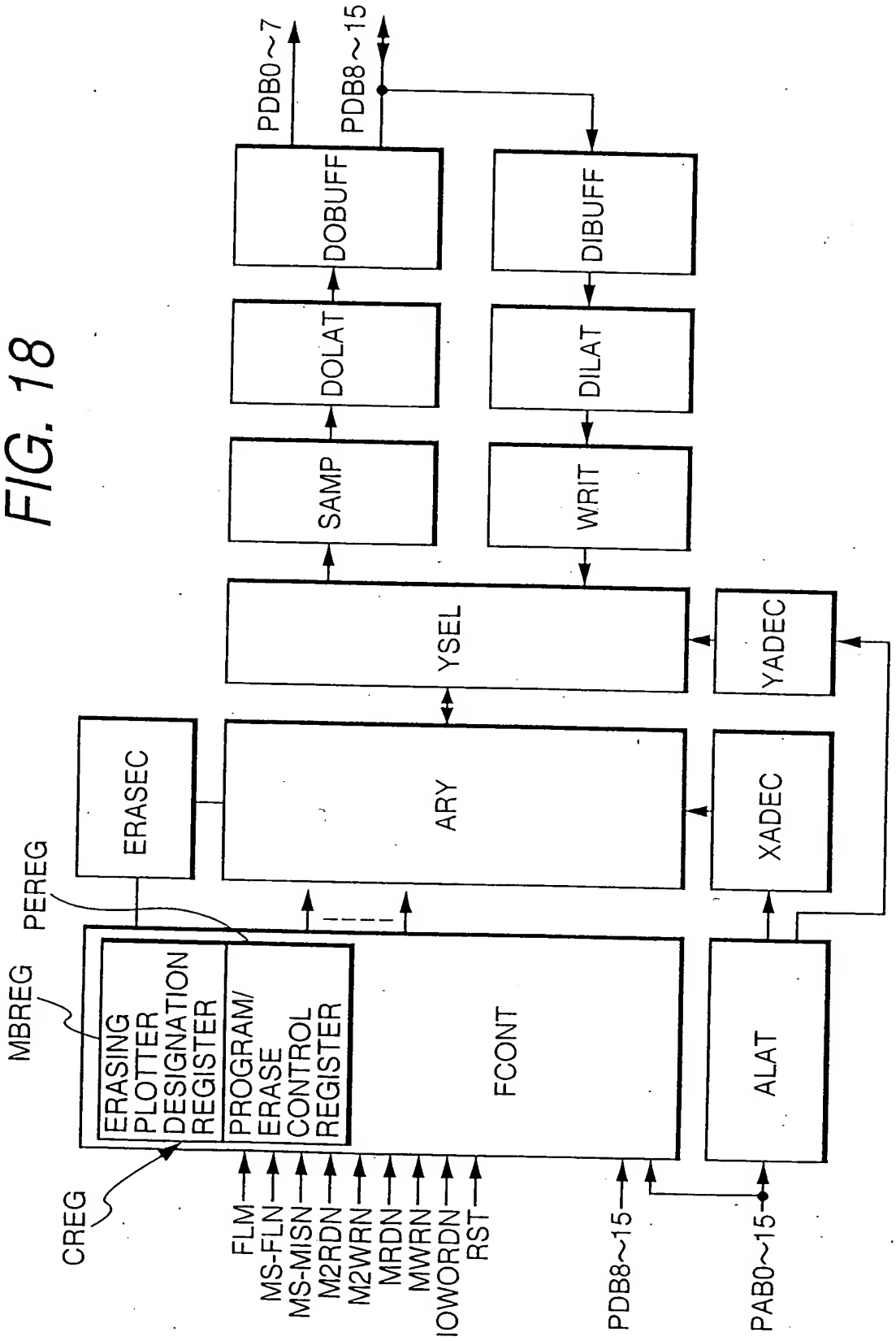
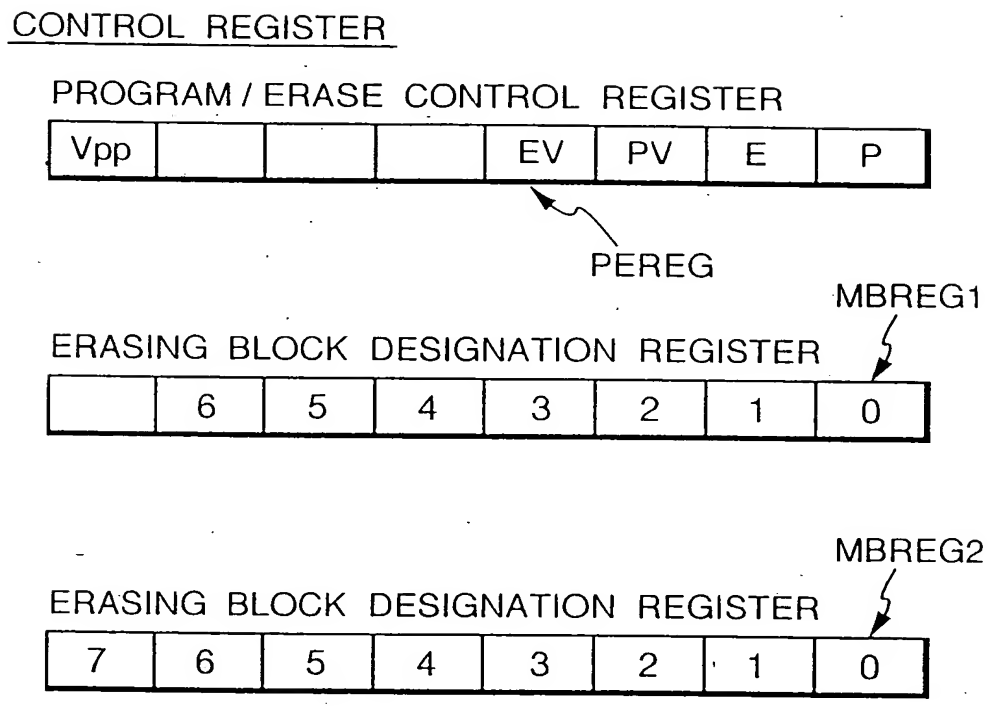


FIG. 19



Vpp : Vpp APPLYING FLAG

E : ERASE
P : PROGRAM

EV : ERASE VERIFY
PV : PROGRAM VERIFY

MBREG1 : FOR DESIGNATION OF LARGE BLOCK
MBREG2 : FOR DESIGNATION OF SMALL BLOCK